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EXAMINER	
BODDIE, WILLIAM	
ART UNIT	**PAPER NUMBER**
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/756,939	PARK, JIN-HO	
	Examiner	Art Unit	
	William L. Boddie	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In an amendment dated, November 26th, 2007, the Applicant amended claims 1, 5, 7 and 11-12. Currently claims 1-14 are pending.

Response to Arguments

2. Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection. Specifically all of the Applicant's arguments are directed to new limitations and are believed to be answered by new rejection grounds which follow.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 12-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kawaguchi et al. (US 5,592,199).

With respect to claim 12, Kawaguchi discloses, an LCD apparatus comprising:

an LCD panel (20 in fig. 1) including gate lines (x-axis 3 in fig. 1, for example) receiving a gate driving signal;

a data driver coupled to the LCD panel (3 y-axis ICs, 5 in fig. 1);

a gate driver coupled to the LCD panel (2 x-axis ICs, 5 in fig. 1);

a timing controller coupled (8 in fig. 1; col. 23, lines 29-40) to the gate driver and to the data driver; and

an output instruction signal line (73 in fig. 1) formed on the LCD panel, the output instruction signal line electrically connecting the timing controller with the data and gate drivers (col. 19, lines 15-18; details the timing control board supplying signal along the circuitry of the device to the drivers. The output instruction signal line is one part of this circuitry and as such is seen as electrically connecting the timing controller with the data and gate drivers);

wherein the gate line and the output instruction signal line are disposed substantially parallel to each other (gate lines are seen as the parallel lines that are output from 2 x-axis ICs, 5 in fig. 1, into the panel, while the output instruction signal lines are seen as the 73 wiring that connects the y-axis ICs; should be clear from fig. 1 that these two sets of lines are parallel to one another) on the same substrate (fig. 3); and

wherein the output instruction signal line is substantially a same length as the gate lines (from figs. 2-3, it is clear that 73 spans substantially the entire length of the LCD panel just as the gate lines do).

With respect to claim 13, Kawaguchi discloses, the LCD apparatus of claim 12 (see above), wherein the output instruction signal line is formed on an area adjacent to the data driver (clear from fig. 1).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawaguchi et al. (US 5,592,199) in view of Kubota et al. (US 6,791,526).

With respect to claim 1, Kawaguchi discloses, an LCD apparatus comprising:

an LCD panel (20 in fig. 1) including gate lines (x-axis 3 in fig. 1, for example) receiving a gate driving signal and a output instruction signal line (73 in figs. 1-3) transmitting an output instruction signal, and displaying an image;

a data driver (3 y-axis ICs, 5 in fig. 1) outputting the image data to the LCD panel;

a gate driver (2 x-axis ICs, 5 in fig. 1) outputting a gate driving signal to the LCD panel; and

a timing controller (8 in fig. 1; col. 19, lines 15-18) providing a first control signal (x-axis 73 in fig. 1) to the gate driver so as to control an output of the gate driving signal and providing the output instruction signal (y-axis 73 in fig. 1) to the data driver via the output instruction signal line so as to control an output of the image data (col. 25, lines 3-12),

wherein the gate line and the output instruction signal line are disposed substantially parallel to each other (gate lines are seen as the parallel lines that are output from 2 x-axis ICs, 5 in fig. 1, into the panel, while the output instruction signal lines are seen as the 73 wiring that connects the y-axis ICs; should be clear from fig. 1 that these two sets of lines are parallel to one another) on the same substrate (fig. 3), and

wherein the output instruction signal line is substantially a same length as the gate lines (from figs. 2-3, it is clear that 73 spans substantially the entire length of the LCD panel just as the gate lines do).

Kawaguchi does not expressly disclose, that the timing of the output of image data is according to a delay of the gate driving signal.

Kubota discloses, that the timing of the output of image data (input and shift register waveforms in fig. 18) is according to a delay of a gate driving signal (output in fig. 18).

Kubota and Kawaguchi are analogous art because they are both from the same field of endeavor namely control circuitry design for LCD panels.

At the time of the invention it would have been obvious to one of ordinary skill in the art to time the gate and data signals of Kawaguchi in the conventional manner disclosed by Kubota.

The motivation for doing so would have been so that each pixel receives the correct data waveform at the appropriate time, as well as for a decreased timing complexity.

With respect to claim 2, Kawaguchi and Kubota disclose, the LCD apparatus of claim 1 (see above).

Kawaguchi further discloses, wherein the output instruction signal line is formed on an area adjacent to the data driver (clear from fig. 1).

With respect to claim 3, Kawaguchi and Kubota disclose, the LCD apparatus of claim 2 (see above).

Kawaguchi further discloses, comprising a plurality of signal transmission members (45 and 3 in fig. 3; for example) electrically connecting the data driver with the LCD panel,

wherein the output instruction signal line receives the output instruction signal from timing controller via one of the signal transmission members (clear from figs. 1-2).

With respect to claim 4, Kawaguchi and Kubota disclose, the LCD apparatus of claim 3 (see above).

Kawaguchi further discloses, wherein the LCD panel comprises:

the gate lines (note the outputting gate lines from the y-axis ICs in fig. 1) receiving the gate driving signal via the gate driver, the gate lines disposed on the LCD panel, extended in a first direction and arranged in a second direction substantially perpendicular to the first direction (fig. 1); and

a plurality of data lines (x-axis 3 in fig. 1) receiving the image data via the data driver, the data lines disposed on the LCD panel, extended in the second direction and arranged in the first direction (col. 37, lines 29-42, discusses the orientation and design of a matrix panel using the gate and data lines oriented in the way currently claimed).

With respect to claim 5, Kawaguchi and Kubota disclose, the LCD apparatus of claim 4 (see above).

Kawaguchi further discloses, wherein the output instruction signal line is extended in the first direction and is substantially parallel to the gate lines (seems clear from figs. 1-3).

With respect to claim 6, Kawaguchi and Kubota disclose, the LCD apparatus of claim 4 (see above).

Kawaguchi further discloses, wherein the LCD panel comprises a plurality of pixel areas defined by the gate and data lines (col. 37, lines 29-42).

Kawaguchi is silent on the exact timing of the signals and their application to pixel areas.

The conventional timing of LCD panel signals is disclosed by Kubota. Kubota discloses, that the gate driving signal is provided to a corresponding pixel area at a same time as that of the image data provided to the corresponding pixel area (col. 1, lines 62-67).

At the time of the invention it would have been obvious to one of ordinary skill in the art to time the gate and data signals of Kawaguchi in the conventional manner disclosed by Kubota.

The motivation for doing so would have been so that each pixel receives the correct data waveform at the appropriate time, as well as for a decreased timing complexity.

With respect to claim 7, Kawaguchi discloses, an LCD apparatus comprising:

an LCD panel (20 in fig. 1) including gate lines (y-axis 3 in fig. 1; for example) receiving a gate driving signal and a output instruction signal line (73 in figs. 1-3) transmitting an output instruction signal, and displaying an image;

a data driver (3 y-axis ICs, 5 in fig. 1) outputting the image data to the LCD panel;

a gate driver (2 x-axis ICs, 5 in fig. 1) outputting a gate driving signal to the LCD panel; and

a timing controller (8 in fig. 1; col. 19, lines 15-18) providing a first control signal (x-axis 73 in fig. 1) to the gate driver so as to control an output timing of the gate driving signal and providing the output instruction signal (y-axis 73 in fig. 1) to the data driver so as to control an output timing of the image data; and

a plurality of signal transmission members (45 and 3 in fig. 3; for example) electrically connecting the data driver with the LCD panel;

wherein the output instruction signal line provides the output instruction signal to the data driver via one of the signal transmission members (clear from figs. 1-3); and

wherein the gate line and the output instruction line are disposed substantially parallel to each other (gate lines are seen as the parallel lines that are output from y-axis ICs in fig. 1 into the panel, while the output instruction signal lines are seen as the 73 wiring that connects the ICs; should be clear from fig. 1 that these two sets of lines are parallel to one another) on the same substrate (fig. 3), and

wherein the output instruction signal line is substantially a same length as the gate lines (from figs. 2-3, it is clear that 73 spans substantially the entire length of the LCD panel just as the gate lines do).

Kawaguchi does not expressly disclose, that the timing of the output of image data is according to a delay of the gate driving signal.

Kubota discloses, that the timing of the output of image data (input and shift register waveforms in fig. 18) is according to a delay of a gate driving signal (output in fig. 18).

At the time of the invention it would have been obvious to one of ordinary skill in the art to time the gate and data signals of Kawaguchi in the conventional manner disclosed by Kubota.

The motivation for doing so would have been so that each pixel receives the correct data waveform at the appropriate time, as well as for a decreased timing complexity.

With respect to claim 8, Kawaguchi and Kubota disclose, the LCD apparatus of claim 7 (see above).

Kawaguchi further discloses, wherein the LCD panel comprises:

the gate lines (note the outputting gate lines from the ICs in fig. 1) extended in a first direction and arranged in a second direction substantially perpendicular to the first direction; and

a plurality of data lines (x-axis 3 in fig. 1) extended in the second direction and arranged in the first direction (col. 37, lines 29-42, discusses the orientation and design of a matrix panel using the gate and data lines oriented in the way currently claimed).

With respect to claim 9, Kawaguchi and Kubota disclose, the LCD apparatus of claim 8 (see above).

Kawaguchi further discloses, wherein the output instruction line is extended in the first direction (clear from fig. 1).

With respect to claim 10, Kawaguchi and Kubota disclose, the LCD apparatus of claim 9 (see above).

Kawaguchi further discloses, wherein the LCD panel comprises a plurality of pixel areas defined by the gate and data lines (col. 37, lines 29-42).

Kawaguchi is silent on the exact timing of the signals and their application to pixel areas.

The conventional timing of LCD panel signals is disclosed by Kubota. Kubota discloses, that the gate driving signal and the image data are substantially simultaneously provided to a corresponding pixel area (col. 1, lines 62-67).

At the time of the invention it would have been obvious to one of ordinary skill in the art to time the gate and data signals of Kawaguchi in the conventional manner disclosed by Kubota.

The motivation for doing so would have been so that each pixel receives the correct data waveform at the appropriate time, as well as for a decreased timing complexity.

With respect to claim 11, Kawaguchi and Kubota disclose, the LCD apparatus of claim 7 (see above).

Kawaguchi further discloses, wherein the signal line is formed on the LCD panel and adjacent to the data driver (clear from fig. 1).

With respect to claim 14, Kawaguchi discloses, the LCD apparatus of claim 13 (see above), further comprising a plurality of signal transmission members (45 and 3 in fig. 3; for example) electrically connecting the data driver with the LCD panel,

wherein the output instruction signal line receives a control signal from the timing controller via one of the signal transmission members so as to control an output of an image data from the data driver (col. 23, lines 29-40; clear from figs. 1-2).

Kawaguchi does not expressly disclose, that the timing of the output of image data is according to a delay of the gate driving signal.

Kubota discloses, that the timing of the output of image data (input and shift register waveforms in fig. 18) is according to a delay of a gate driving signal (output in fig. 18).

At the time of the invention it would have been obvious to one of ordinary skill in the art to time the gate and data signals of Kawaguchi in the conventional manner disclosed by Kubota.

The motivation for doing so would have been so that each pixel receives the correct data waveform at the appropriate time, as well as for a decreased timing complexity.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Will L. Boddie whose telephone number is (571) 272-0666. The examiner can normally be reached on M-F, 7:30 - 4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

2/13/08
wlb

Sumati Lefkowitz

SUMATI LEFKOWITZ
SUPERVISORY PATENT EXAMINER